What Is Claimed Is:

1. A semiconductor module comprising:

a module board having a support body on an upper surface thereof and external electrode terminals on a lower surface thereof;

a first semiconductor chip fixed to the module board in a posture that electrodes formed over a main surface are formed over an upper side of the semiconductor chip;

a second semiconductor chip having a portion thereof overlapped to and above the first semiconductor chip in plane such that the second semiconductor chip is not brought into contact with the first semiconductor chip, the second semiconductor chip being supported by and fixed to the support body; and

conductive wires electrically connecting the first semiconductor chip and the module board.

2. The semiconductor module according to claim 1, wherein a portion of the support body is formed of a conductor.

3. The semiconductor module according to claim 2, wherein vias which are formed of a conductor and penetrate between the upper and lower surfaces of the module board are formed in the module board, and the support body formed of the conductor is connected to the vias.

4. The semiconductor module according to claim 1, wherein the support body assumes a reference potential.

5. The semiconductor module according to claim 2, wherein the first semiconductor chip and the second semiconductor chip are electrically connected to each other through the support body.

6. The semiconductor module according to claim 1, wherein the support body is formed of a projection which is formed together at the time of forming the module board.

7. The semiconductor module according to claim 6, wherein vias which are formed of a conductor and penetrate between the upper and lower surfaces of the module board are formed inside the support body.

8. The semiconductor module according to claim 1, wherein the support body constitutes a separate part with respect to the module board and is fixed to the module board.

9. The semiconductor module according to claim 8, wherein the support body is formed of a ball.

10. The semiconductor module according to claim 9, wherein the support body is formed of the conductor and is electrically connected with vias formed of a conductor which penetrate between the upper and lower surfaces of the module board.

11. The semiconductor module according to claim 1, wherein vias which are formed of a conductor and penetrate between the upper and lower surfaces of the module board are formed in the module board, a heat radiation pad formed of a

conductive layer is formed over the lower surface of the module board, and the vias are connected to the heat radiation pad.

12. The semiconductor module according to claim 1, wherein one side of the second semiconductor chip is longer than one side of the first semiconductor chip.

13. The semiconductor module according to claim 1, wherein a heat value of the first semiconductor chip is larger than a heat value of the second semiconductor chip.

14. The semiconductor module according to claim 1, wherein vias which are formed of a conductor and penetrate between the upper and lower surfaces of the module board are formed in the module board, and the first semiconductor chip is connected to the vias.

15. The semiconductor module according to claim 1, wherein the first semiconductor chip and the second semiconductor chip are connected to a common reference potential electrode.

16. The semiconductor module according to claim 1, wherein a recess is formed in the upper surface of the module board and the first semiconductor chip is fixed to a bottom of the recess.

17. The semiconductor module according to claim 16, wherein vias formed of a conductor which penetrate between the upper and lower surfaces of the module board are formed in the bottom of the recess, a heat radiation pad formed of a conductive

layer is formed over the lower surface of the module board, and the vias are connected to the heat radiation pad.

18. The semiconductor module according to claim 1, wherein a reference potential electrode is formed over a lower surface of the second semiconductor chip.

19. The semiconductor module according to claim 1, wherein a reference potential electrode is formed over a lower surface of the first semiconductor chip.

20. The semiconductor module according to claim 1, wherein electrodes formed over an upper surface of the second semiconductor chip and wiring formed over the module board are electrically connected to each other by conductive wires.

21. The semiconductor module according to claim 1, wherein an upper surface of the support body is set higher than a loop height of the wires connected to the first semiconductor chip.

22. The semiconductor module according to claim 1, wherein a recess is formed in the upper surface of the module board, the support body is formed over the upper surface of the module board around the recess, the first semiconductor chip is fixed to a bottom of the recess, the second semiconductor chip is fixed to the support body, and an upper surface of the support body is set higher than a loop height of the wires connected to the first semiconductor chip.

23. The semiconductor module according to claim 1,

wherein active elements are formed over the first semiconductor chip and the second semiconductor chip respectively, and the active element of the first semiconductor chip and another active element included in the second semiconductor chip are controlled based on the active element of the second semiconductor chip.

24. The semiconductor module according to claim 23, wherein the semiconductor module includes a power amplifying device to which a plurality of transistors are connected based on cascade connection in a multiple stages, and a first-stage transistor of the power amplifying device is included in the second semiconductor chip, and a final-stage transistor of the power amplifying device is included in the first semiconductor chip.

25. A semiconductor module in which the semiconductor module according to claim 24 is a semiconductor module mounted on a mobile telephone.

26. The semiconductor module according to claim 1, further comprising passive parts.

27. The semiconductor module according to claim 1, wherein the first and the second semiconductor chips, the support body, the wires and the electronic parts are covered with a sealing portion made of resin having an insulation property.

28. The semiconductor module according to claim 27,

wherein end portions of the sealing portion are not positioned outside end portions of the module board.

29. The semiconductor module according to claim 27, wherein the resin which forms the sealing portion is a silicone resin which has the Young's modulus of 1 to 200 Mpa and a thermal expansion coefficient α of 180×10^{-6}/°C to 200×10^{-6}/°C or an epoxy resin which has the Young's modulus of 1000 to 10000 Mpa.

30. A semiconductor module comprising:

a module board having a support body formed of a conductor on an upper surface thereof and external electrode terminals on a lower surface thereof;

a first semiconductor chip fixed to the module board in a posture that electrodes formed over a main surface are formed over an upper side of the first semiconductor chip;

a second semiconductor chip overlapped to and above the first semiconductor chip with a gap therebetween and fixed to the support body;

conductive wires electrically connecting the first and the second semiconductor chips with the module board; and

electronic parts electrically connected to the module board, wherein

transistors are provided to the first semiconductor chip and the second semiconductor chip respectively, a high frequency power amplifying device is constituted by multi-stage cascade connection of the transistors, a first-stage transistor

of the high frequency power amplifying device is included in the second semiconductor chip, and a final-stage transistor of the high frequency power amplifying device is included in the first semiconductor chip, and

wherein a reference potential layer is formed over a lower surface of the second semiconductor chip and the support body is connected to the reference potential layer.